MASTER/SLAVE WORLDFIP BUS CONTROLLER

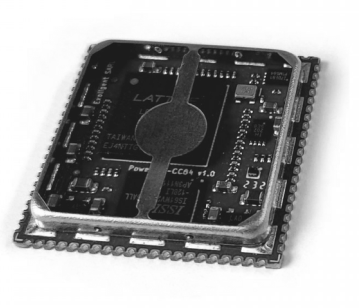
SEPTEMBER 2024

1 Features

- WorldFIP/FIP protocol services
  - Slave or Master (Bus Arbiter) station
  - Periodic/Aperiodic variables
  - Periodic/Aperiodic messages
  - SM-MPS support
  - Bitrate support : 31.25Kbps, 1Mbps, 2.5Mbps, 5Mbps
  - Medium redundancy : Mono-/Bi-medium
- Line driver chips support
  - Alstom's FielDrive™
  - Exoligent's FipDrive™
  - Generic RS-485 drivers
- LVTTL compatible inputs and outputs
- Host Interface
  - 8-/16-/32-bit Dual Port Memory (DPM)
  - Multiplexed/Non-multiplexed modes
  - Synchronous/Asynchronous modes
- 4MB private memory
- Handle up to 4096 identifiers
- Single power supply
  - 2.4V-3.3V VDD
- Dimensions (L x W x H)
  - 29.21 x 29.21 x 4 mm
- Contacting / Pinout
  - 84 solder contacts 1mm with 1.27mm grid
  - PLCC-84 footprint compliant
- Operating temperature
  - -40°C to +85°C
- Lead-free available
- Designed in France

3 Applications

- PLC
- I/O Mux
- Motor drives
- Console
- Factory automation & control



2 Description

The *EXOLIGENT* POWERFIP-CC Chip Carrier is a real-time communication controller for WorldFIP fieldbus.
WorldFIP is a deterministic fieldbus used for the exchange of data between the sensors/actuators, and the control/supervision level. This chip implements most of the link and application of the protocol (IEC 61158).

Soldered directly to the host system, POWERFIP-CC provides a fast and safe alternative for developing a master/slave WorldFIP node. It offers a variety of host interfaces, which makes it compatible with a wide range of microcontrollers/microprocessors avoiding external logic glue devices.

The chip supports medium redundancy management, allowing two FIP line transceivers to be connected to it.

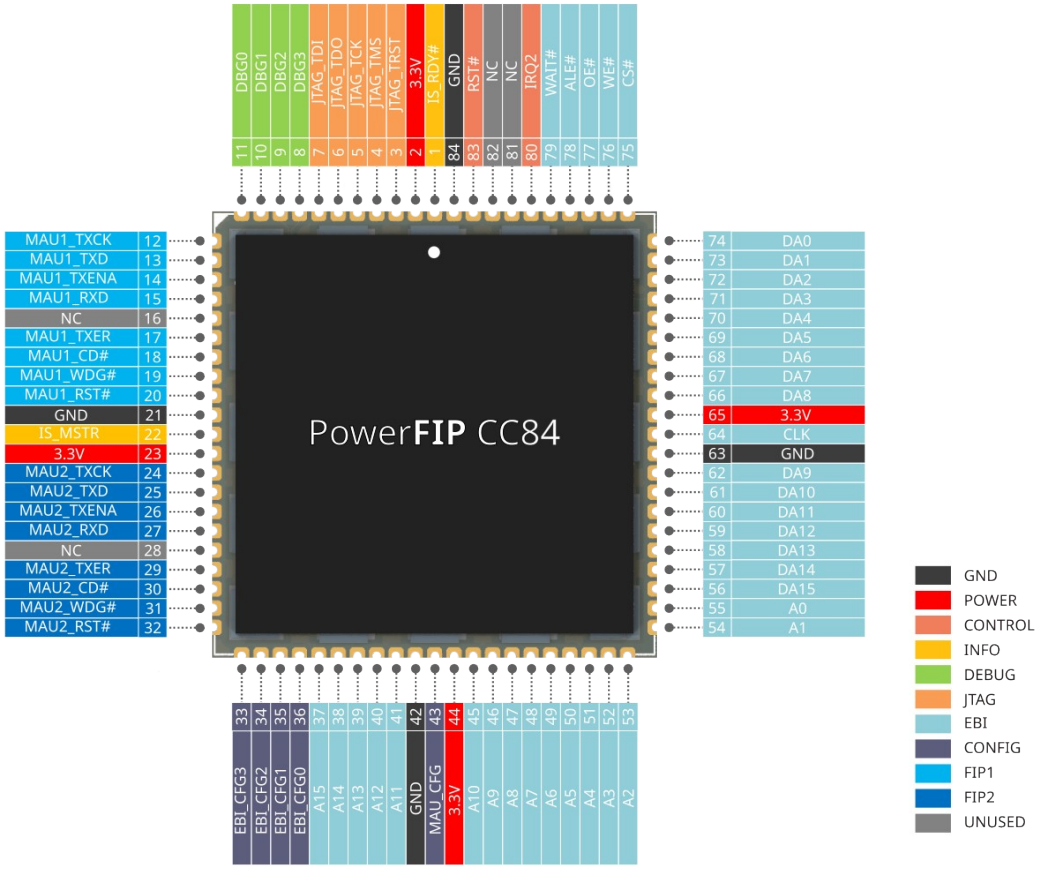
This chip carrier is 3.3V single-rail power supplied and is optimized for minimum footprint including : FPGA, 32Mb SRAM, 16Mb FLASH NOR, UID/Temperature IC, 1V/1V8 regulators, 20MHz clock oscillator.

Table of Contents

4 Revision History

Revision	Changes	Authors	Date
Rev.A to Rev.B	Add: *Timing Considerations* Section Add: *Read/Write Performance* Section Fix: *Memory Area Descriptions* Section (Mailbox Area)	MC	9/24
Rev.A	Initial Version	MC	7/24

5 Pin Configuration and Functions



Pin Descriptions

Pin Number	Pin Name	Type	Description
1	IS_RDY#	O	Chip is ready (else, is booting)
2	VCC3V3	PWR	Positive supply voltage (+3.3V)
3	JTAG_TRST	I	JTAG – Test Reset
4	JTAG_TMS	I	JTAG – Test Mode Select
5	JTAG_TCK	I	JTAG – Test Clock
6	JTAG_TDO	O	JTAG – Test Data Out
7	JTAG_TDI	I	JTAG – Test Data In
8	DBG3	O	Debug 3 output (MAU1_TXER)
9	DBG2	O	Debug 2 output (MAU1_CD#)
10	DBG1	O	Debug 1 output (MAU1_RXD)
11	DBG0	O	Debug 0 output (MAU1_TXD)

Pin Number	Pin Name	Type	Description
12	MAU1_TXCK	O	Half bit clock[1] (line driver 1)
13	MAU1_TXD	O	Transmitter data (line driver 1)
14	MAU1_TXENA	O	Transmitter enable (line driver 1)
15	MAU1_RXD	I	Received data (line driver 1)
16	NC	I	Reserved (note: MAU1_ACT)
17	MAU1_TXER	I/O	Transmitter error (line driver 1)
18	MAU1_CD#	I/O	Reception activity detection (line driver 1)
19	MAU1_WDG#	I/O	Watchdog on transmitter (line driver 1)
20	MAU1_RST#	O	Initialization control (line driver 1)
21	GND	PWR	Negative supply voltage (0V)
22	IS_MSTR	O	Bus Arbiter activity
23	VCC3V3	PWR	Positive supply voltage (+3.3V)
24	MAU2_TXCK	O	Half bit clock[1] (line driver 2)
25	MAU2_TXD	O	Transmitter data (line driver 2)
26	MAU2_TXENA	O	Transmitter enable (line driver 2)
27	MAU2_RXD	I	Received data (line driver 2)
28	NC	I	Reserved (note: MAU2_ACT)
29	MAU2_TXER	I/O	Transmitter error (line driver 2)
30	MAU2_CD#	I/O	Reception activity detection (line driver 2)
31	MAU2_WDG#	I/O	Watchdog on transmitter (line driver 2)
32	MAU2_RST#	O	Initialization control (line driver 2)
33	EBI_CFG3	I	External Bus Interface mode selection
34	EBI_CFG2	I	External Bus Interface mode selection
35	EBI_CFG1	I	External Bus Interface mode selection
36	EBI_CFG0	I	External Bus Interface mode selection
37	A15	I	Demultiplexed address bus
38	A14	I	Demultiplexed address bus
39	A13	I	Demultiplexed address bus
40	A12	I	Demultiplexed address bus
41	A11	I	Demultiplexed address bus
42	GND	PWR	Negative supply voltage (0V)
43	MAU_CFG	I	Line driver mode selection
44	VCC3V3	PWR	Positive supply voltage (+3.3V)

Pin Number	Pin Name	Type	Description
45	A10	I	Demultiplexed address bus
46	A9	I	Demultiplexed address bus
47	A8	I	Demultiplexed address bus
48	A7	I	Demultiplexed address bus
49	A6	I	Demultiplexed address bus
50	A5	I	Demultiplexed address bus
51	A4	I	Demultiplexed address bus
52	A3	I	Demultiplexed address bus
53	A2	I	Demultiplexed address bus
54	A1	I	Demultiplexed address bus
55	A0	I	Demultiplexed address bus
56	DA15	I/O	Multiplexed address-data bus
57	DA14	I/O	Multiplexed address-data bus
58	DA13	I/O	Multiplexed address-data bus
59	DA12	I/O	Multiplexed address-data bus
60	DA11	I/O	Multiplexed address-data bus
61	DA10	I/O	Multiplexed address-data bus
62	DA9	I/O	Multiplexed address-data bus
63	GND	PWR	Negative supply voltage (0V)
64	CLK	I	EBI clock (Synchronous mode)
65	VCC3V3	PWR	Positive supply voltage (+3.3V)
66	DA8	I/O	Multiplexed address-data bus
67	DA7	I/O	Multiplexed address-data bus
68	DA6	I/O	Multiplexed address-data bus
69	DA5	I/O	Multiplexed address-data bus
70	DA4	I/O	Multiplexed address-data bus
71	DA3	I/O	Multiplexed address-data bus
72	DA2	I/O	Multiplexed address-data bus
73	DA1	I/O	Multiplexed address-data bus
74	DA0	I/O	Multiplexed address-data bus
75	CS#	I	EBI Chip Select
76	WE#	I	EBI Write Strobe (Writing signal from µC)
77	OE#	I	EBI Read Strobe (Reading signal from µC)

Pin Number	Pin Name	Type	Description
78	ALE#	I	EBI Address Latch Enable (Address validation)
79	WAIT#	O	EBI Wait Signal (Chip communication is busy)
80	IRQ2	O	Interrupt Request 2 (Mailbox 2)
81	NC	O	Reserved (note: IRQ1)
82	NC	O	Reserved (note: IRQ0)
83	RST#	I	Reset (Circuit initialization)
84	GND	PWR	Negative supply voltage (0V)

Notes:

1. ex : 2MHz@1Mbps

6 Specifications

6.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	-0.5	3.63	V
V_{IN}	Input Voltage	-0.5	V_{DD} + 0.3	V
T_{stg}	Storage Temperature	-65	+150	°C
T_{amb}	Ambient Temperature	-40	+85	°C
T_J	Junction Temperature	-	+125	°C

Notes:

- Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All voltages referenced to GND.

6.2 Recommended Operating Conditions

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.135	3.30	3.465	V
V_{IN}	Input Voltage	0	-	V_{DD}	V
T_{amb}	Ambient Temperature (in free air)	-40	-	+85	°C
T_J	Junction Temperature	-40	-	+100	°C

6.3 Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage		-	-	0.8	V
V_{IH}	High-level input voltage		2.0	-	V_{DD} + 0.3	V
V_{OL}	Low-level ouput voltage		-	-	0.4	V
V_{OH}	High-level output voltage		V_{DD} - 0.4	-	-	V
I_{OL}	Low-level ouput current		2	-	-	mA
I_{OH}	High-level output current		-	-	-2	mA
I_{IL}, I_{IH}[1]	Input or I/O Leakage current	$0 \le V_{IN} \le V_{DD}$	-	-	10	µA
I_{IH}[2]	Input or I/O Leakage current	$V_{DD} \le V_{IN} \le V_{IH}$ (max)	-	-	100	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7 \times V_{DD}$	-30	-	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (max) $\le V_{IN} \le V_{DD}$	30	-	150	µA
C_{IN}[3]	I/O Capacitance	V_{DD} = 3.3V, V_{IO} = 0 to V_{DD} + 0.2V	-	6	-	pF

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.
2. The input leakage current I_{IH} is the worst case input leakage per GPIO when the pad signal is high and also higher than VDD. This is considered a mixed mode input.
3. T_A 25 °C, f = 1.0 MHz.

6.4 Timing Considerations

Symbol	Description	Value	Unit
T_{SU}	Start-Up Time (from Power-On to DPM content valid)	~1.024	s
1 ▸ T_{FW}	Firmware Image Loading Time from QSPI Flash	~684	us
2 ▸ T_{AUTH}	Crypto Authentification Time	~800	ms
3 ▸ T_{OTHER}	SRAM + DPM Initialization Time	~200	ms

7 Detailed Description

7.1 Overview

POWERFIP-CC is a top-side mounted circuit board in the compact dimensions of 29.21x29.21 mm and will be soldered to the baseboard. As for a QFP part the solder pads are located on the side and enables an easy handling. With its integrated WorldFIP stack and an internal 4MB SRAM, this chip carrier is optimized for minimum footprint. Its focus is purely on real-time WorldFIP communication.

Embedded WorldFIP stack implements most of the link and application protocols of the WorldFIP fieldbus :

- Physical Layer :
  - WorldFIP or FIP frames
- Data Link Layer :
  - Variable transfer services
  - Variable updating requests services
  - Message transfer services
- MPS Application Layer :
  - Management of refreshment and promptness statuses
  - Verification of variable type and size
- Network Management :
  - Medium redundancy
  - Error counters and performance on both medium
- Additional functions :
  - Synchronization with specialized interruption
  - Distribution of precise time

This chip is intended to equip any field device having a certain intelligence level such as PLC, I/O Mux, Drive, Console … capable of managing a great number of variables, including intelligent sensors and actuators.

It implements a set of periodic and aperiodic buffer transfer and messaging services of the data link layer, as well as for a station supporting the arbitrator function as for a slave station.

It also supports the MPS application layer services including : promptness, refreshment and synchronizations mechanisms. It can process up to 4096 identifiers among the 65536 possible on the network.

For this chip carrier embeds a private SRAM of 4MB. The objects handled by the circuit which constitutes the local database are stored in this memory address space.

The circuit is microprogrammed. A part of the microprogram is located in an internal NOR Flash while the remaining part is loaded into the internal SRAM.

It is interfaced through a configurable bus (16-bit, 32-bit) with the host processor in charge of running the application software.

To guarantee the external behaviour of the POWERFIP-CC, it is strongly recommended to use the POWERFIP API[1] software which implements the handling sequences to access the chip.

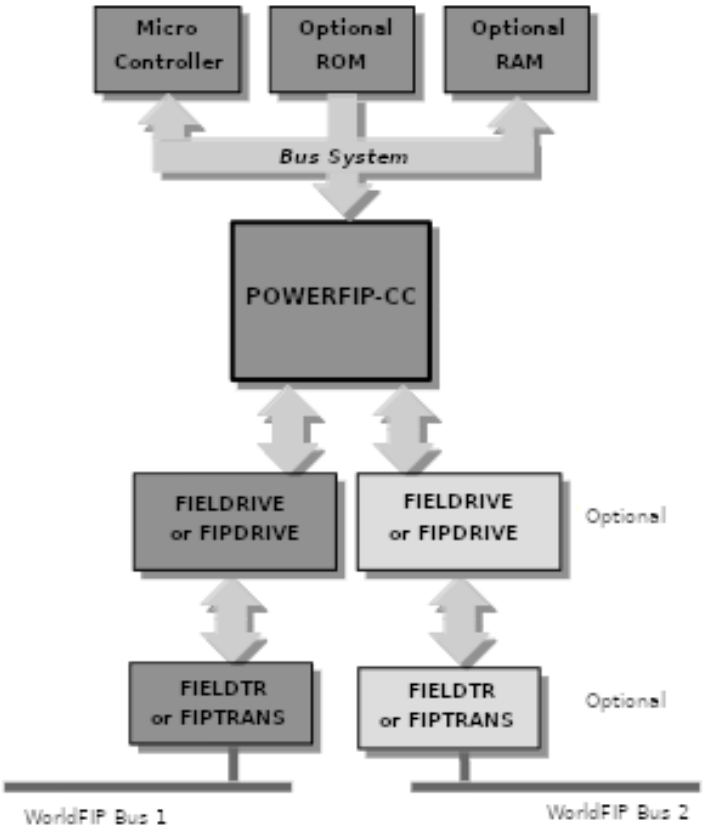
The user requests and the network events may be totally asynchronous as any database access conflict is solved by internal algorithms.

On the network side, POWERFIP-CC is connected to the WorldFIP bus by a line driver which can be doubled to ensure medium redundancy.

This chip implements a FIP standardized full-duplex UART whose transmission rate is selectable among the following values : 31.21Kbps, 1Mbps, 2.5Mbps and 5 Mbps.

The transmit and receive signals on the network interface are encoded data sequence (Manchester Biphase L).

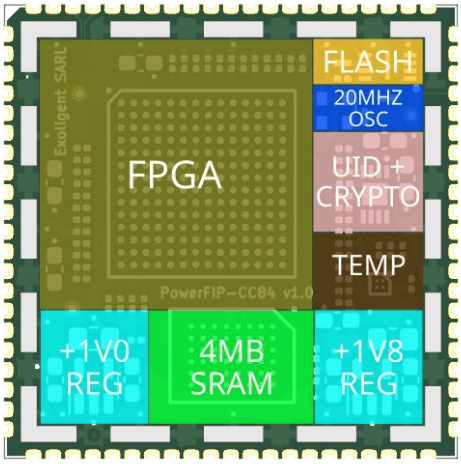
PowerFIP-CC Architecture (Microcontrolled Mode)



Notes:

1. POWERFIP API is a ANSI C library.
   Source code is supplied with the purchase of a POWERFIP-CC-DEVBOARD (STM32 Development Board).

7.2 Feature Description



- **FPGA**

  FPGA is a Lattice Certus-NX (LFD2NX-40-7BG196I) with 39k logic cells. It features a RISCV@100MHz soft-CPU core which manages the essentials of the WorldFIP protocol (configuration, frame scheduling). Some hard real-time critical tasks are allocated to HDL blocks to releave the load on the CPU.

- **FPGA Clock**

  20MHz crystal clock oscillator used to create one clock domain for FPGA (PLL@100MHz).

- **NOR Flash Memory**

  The configuration memory in FPGA is built using volatile SRAM; therefore, an external non-volatile configuration memory is required to maintain the configuration data when the power is removed.

- **SRAM Memory**

  This private memory contains the buffers of produced and consumed variables, the queues of messages waiting for reception or transmission, the bus arbitrator tables (if any).

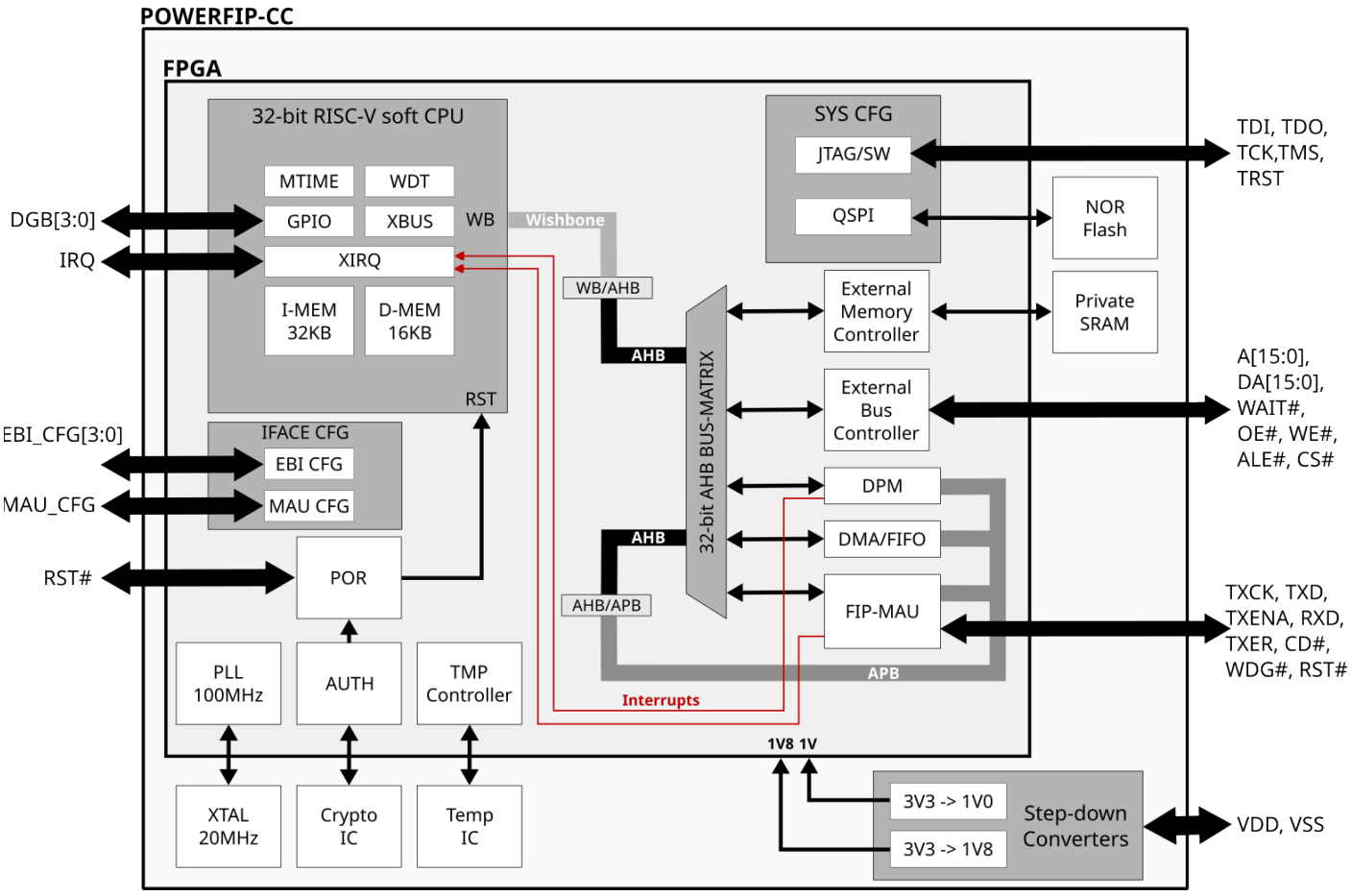
- **Temperature**

  Digital temperature sensor with 12-bit resolution (0.0625°C).

- **UID / Crypto IC**

  Used to provide the chip's unique identifier (48-bit) and protect the FPGA bitstream against unauthorized duplication.

7.3 Functional Block Diagram



7.4 WorldFIP Functional Characteristics

WorldFIP Functions	POWERFIP-CC Capability
Variables Count	4095 128-bytes variables with 4MB of RAM
Request for Aperiodic Variables' Transfer	Supported
Refreshment Status Management	Integrated
Promptness Status Management	Integrated
SM-MPS Variables Management	Identification, Report, Presence, Presence Check, BA Synchronization
Message Transmission Channels' Count	8 Periodic + 1 Aperiodic
Message Reception Queues' Count	1
Message Size	256-bytes
Routing and Broadcasting Management	By software
LSAP Management	By software
Medium Redundancy Management	Integrated
Bus Arbitrator	Supported

8 Host Interface

The data transfer between the circuit and the user processor is handled using an SRAM-like interface with configurable 8-,16-,32-bit data bus width. EBI coupling interface mode selection is performed through dedicated input pins : *EBI_CFG[3..0]*

External Bus Interface Configuration

EBI_CFG[3..0]		
Value - [Binary]	Description	Status
0 - [0000]	Asynchronous 8-bit Non-multiplexed	In Progress
1 - [0001]	Asynchronous 16-bit Multiplexed	Done
2 - [0010]	Asynchronous 16-bit Non-multiplexed	In Progress
3 - [0011]	Asynchronous 32-bit Multiplexed	In Progress
4 - [0100]	Synchronous 8-bit Non-multiplexed	In Progress
5 - [0101]	Synchronous 16-bit Multiplexed	In Progress
6 - [0110]	Synchronous 16-bit Non-multiplexed	In Progress
7 - [0111]	Synchronous 32-bit Multiplexed	In Progress
8 - [1000]	Quad-SPI	In Progress
9 - [1001]	Reserved	-

Notes:

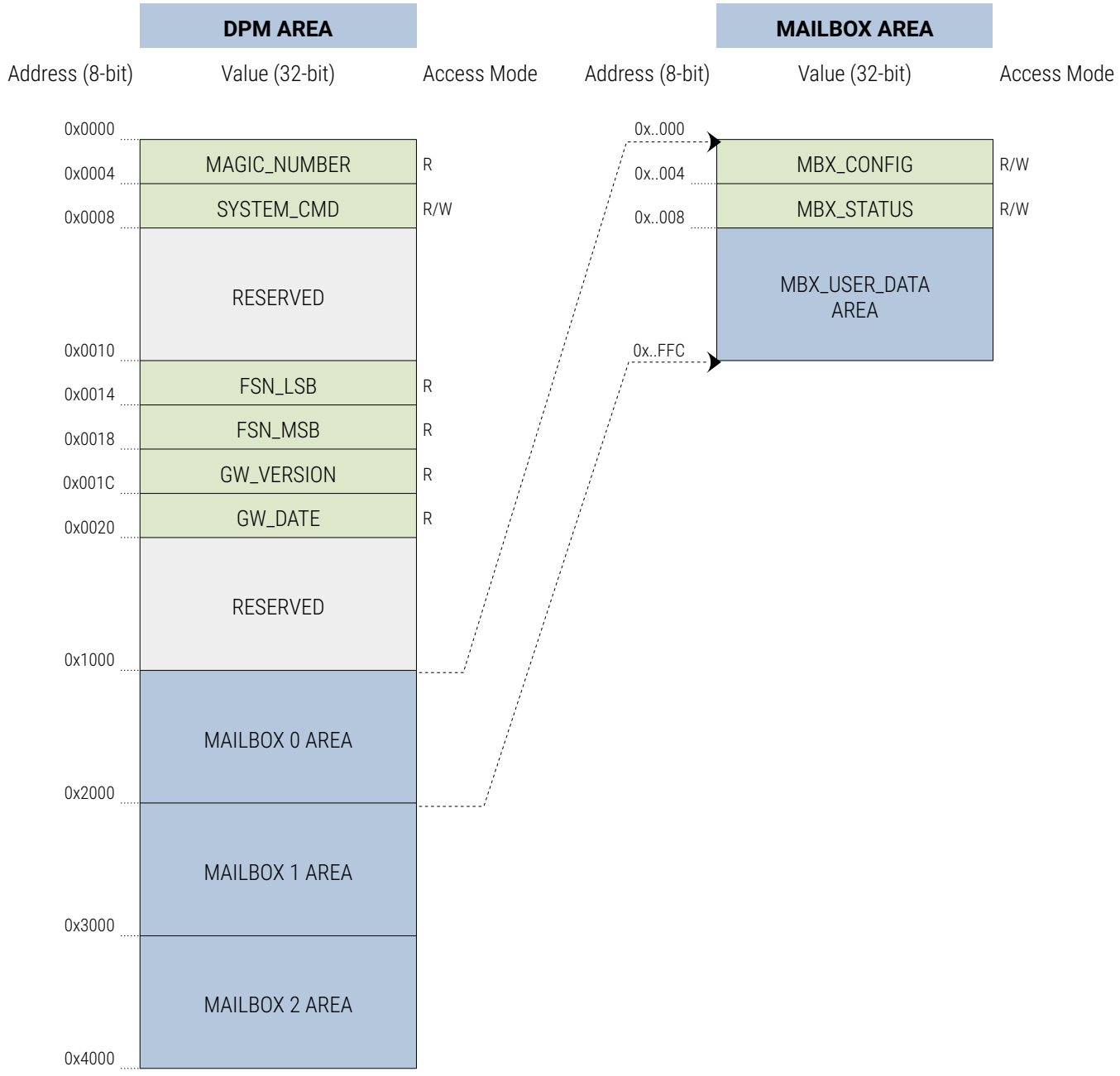
- The chip is hardware-ready for these communication modes. However, the firmware does not yet implement all interfaces. They will be progressively made available in next firmware updates.

8.1 Dual-Port Memory Area

The accessible memory space of the DPM area is organized as described below. It is used to control structured exchanges via mailboxes.

This datasheet only gives an overview of this memory area. It does not describe in detail the structured data for the operation of POWERFIP-CC. Users are strongly advised to use the POWERFIP C API library software developed by EXOLIGENT to carry out exchanges from a host microcontroller.

8.1.1 Memory Area Descriptions



8.1.2 Register Descriptions

MAGIC NUMBER REGISTER

	0x03	0x02	0x01	0x00
MAGIC_NUMBER	0xD1	0xE4	0xCA	0xFE

SYSTEM COMMAND REGISTER

	0x03	0x02	0x01	0x00
SYSTEM_CMD		SINT GINT		GRST CRST

Command Name	Register Bit Number	Access Mode	Value	Description
CRST	b0	R/W	0 : reset - 1 : normal [default]	CC's Soft-CPU Reset
GRST	b1	R/W	0 : reset - 1 : normal [default]	Global Reset (CC's Soft-CPU + Logic)
GINT	b16	R/W	0 : disable [default] - 1 : enable	Mailboxes Global Interrupt
SINT	b17	R/W	0 : disable [default] - 1 : enable	Mailboxes Separated Interrupts

Notes:

- Bits 16 and 17 are exclusive. They cannot both be set at the same time. If they are simultaneously high, then the global interrupt is applied.

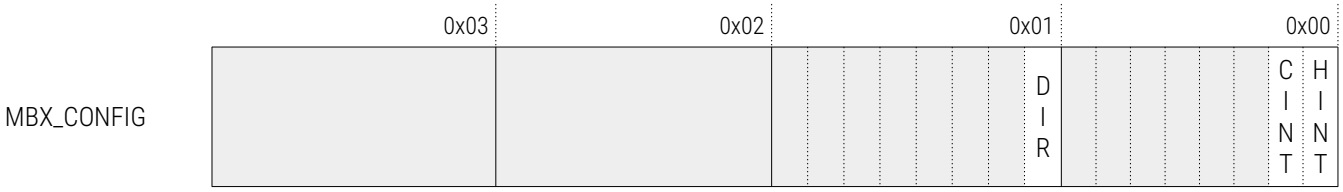
FACTORY SERIAL NUMBER REGISTER

	0x03	0x02	0x01	0x00
FSN_MSB	UID[5]	UID[4]	UID[3]	UID[2]
FSN_LSB	UID[0]	UID[0]	0x01	0x23

GATEWARE INFO REGISTER

	0x03	0x02	0x01	0x00
GW_VERSION	0xAE	Major	Minor	Revision
GW_DATE	0x6C	Year	Month	Day

MAILBOX CONFIG REGISTER

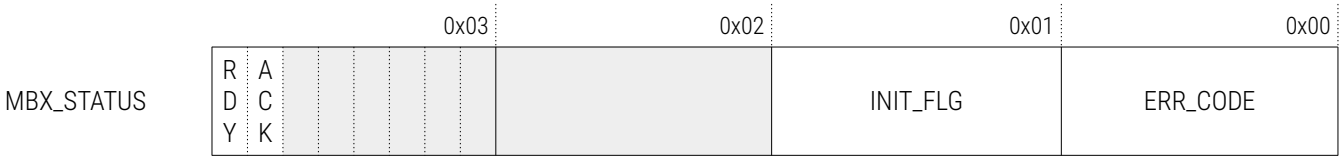


Command Name	Register Bit Number	Access Mode	Value	Description
HINT[1]	b0	R/W	0 : disable [default] - 1 : enable	Host Interrupt Enable
CINT[1]	b1	R/W	0 : disable [default] - 1 : enable	CC's Soft-CPU Interrupt Enable
DIR[2]	b8	R/W	0 : inbox - 1 : outbox	Mailbox Direction

Notes:

1. The interruption is raised when the mailbox buffer is marked as ready (MBX_STATUS register - RDY bit).
2. Depending on the mailbox's direction, the receiving side cannot write and only has access to the reply fields in the MBX_STATUS register.

MAILBOX STATUS REGISTER

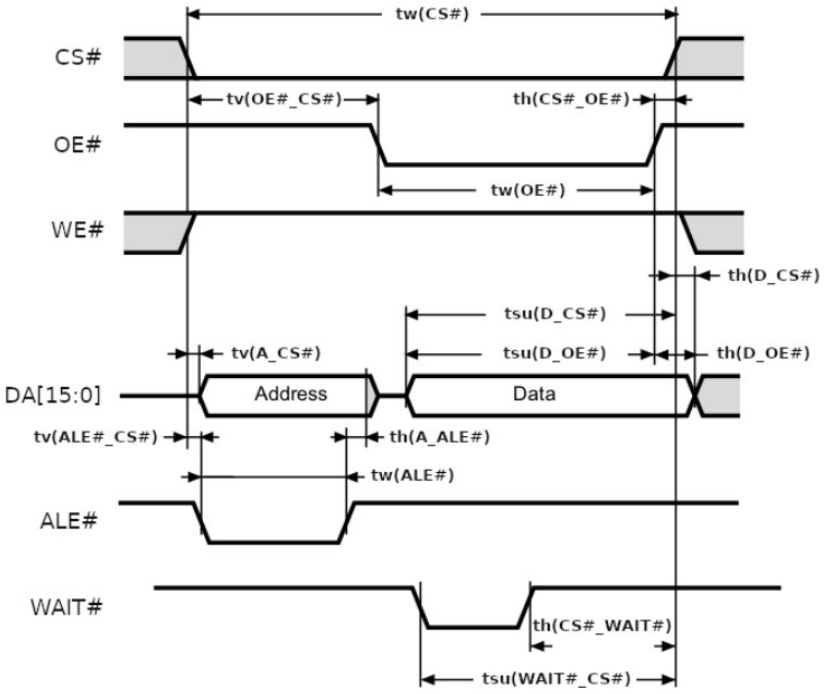


Command Name	Register Bit Number	Access Mode	Value	Description
ERR_CODE	b7-b0	R/W	-	Error code notified by the receiver before acknowledging receipt of a packet (ACK flag).
INIT_FLG	b15-b8	R/W	-	Type of transfer notified by the sender before marking a packet as ready (RDY flag).
ACK	b30	R/W	0 : no - 1 : yes	Acknowledgment flag. Set by the receiver after packet treatment.
RDY	b31	R/W	0 : no - 1 : yes	Ready flag. Set by the sender to signal a new packet.

8.2 External Bus Interface Timing

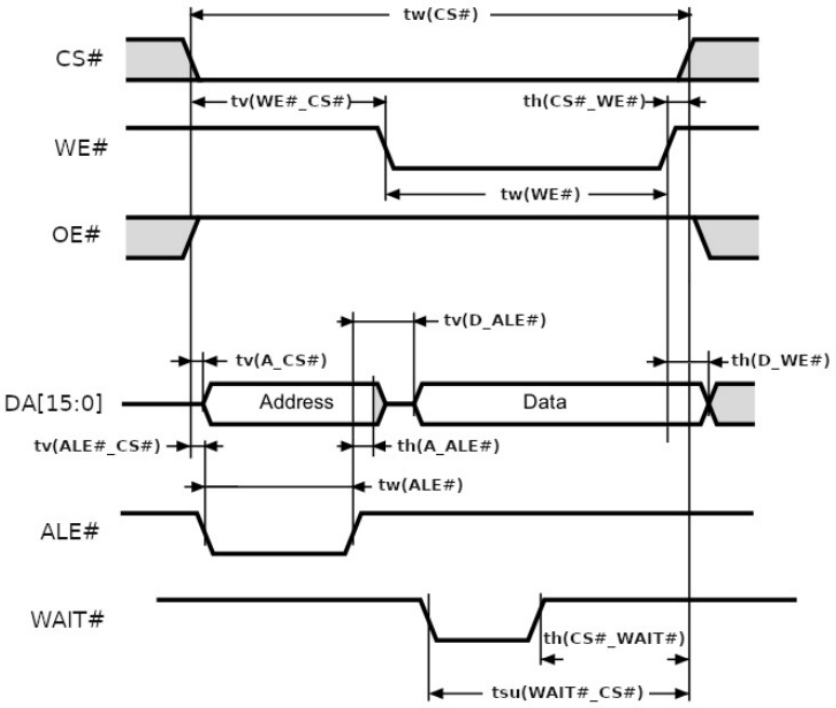
8.2.1 Asynchronous Multiplexed EBI

[READ] Asynchronous Multiplexed Timings[1]



Symbol	Description	Min	Max	Unit
tw(CS#)	CS# low time	169	170	ns
tv(OE#_CS#)	CS# low to OE# low	20	20.5	
tw(OE#)	OE# low time	98.5	100.5	
th(CS#_OE#)	OE# high to CS# high hold time	0	-	
tv(A_CS#)	CS# low to Address valid	-	0.5	
tv(ALE#_CS#)	CS# low to ALE# low	0	0.5	
tw(ALE#)	ALE# low time	49.5	51	
th(A_ALE#)	Address valid hold time after ALE# high	10.5	-	
tsu(D_CS#)	Data to CS# high setup time	11	-	
tsu(D_OE#)	Data to OE# high setup time	11	-	
th(D_CS#)	Data hold time after CS# high	0	-	
th(D_OE#)	Data hold time after OE# high	0	-	
tsu(WAIT#_CS#)	WAIT# valid before CS# high	51	-	
th(CS#_WAIT#)	CS# hold time after WAIT# invalid	41.5	-	

[WRITE] Asynchronous Multiplexed Timings[1]



Symbol	Description	Min	Max	Unit
tw(CS#)	CS# low time	179	180	ns
tv(WE#_CS#)	CS# low to WE# low	9	10.5	
tw(WE#)	WE# low time	119.5	120.5	
th(CS#_WE#)	WE# high to CS# high hold time	9.5	-	
tv(A_CS#)	CS# low to Address valid	-	0	
tv(ALE#_CS#)	CS# low to ALE# low	0	0.5	
tw(ALE#)	ALE# low time	50	51	
th(A_ALE#)	Address valid hold time after ALE# high	10.5	-	
tv(D_ALE#)	ALE# high to Data valid	-	12	
th(D_WE#)	Data hold time after WE# high	10.5	-	
tsu(WAIT#_CS#)	WAIT# valid before CS# high	61	-	
th(CS#_WAIT#)	CS# hold time after WAIT# invalid	51.5	-	

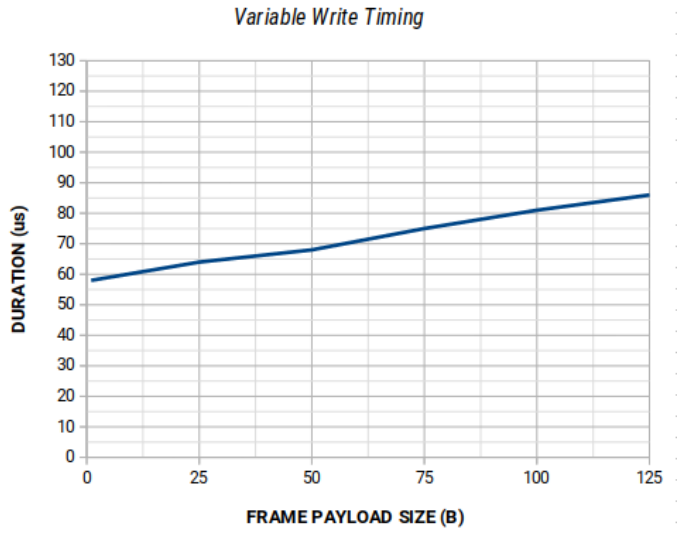
Notes:

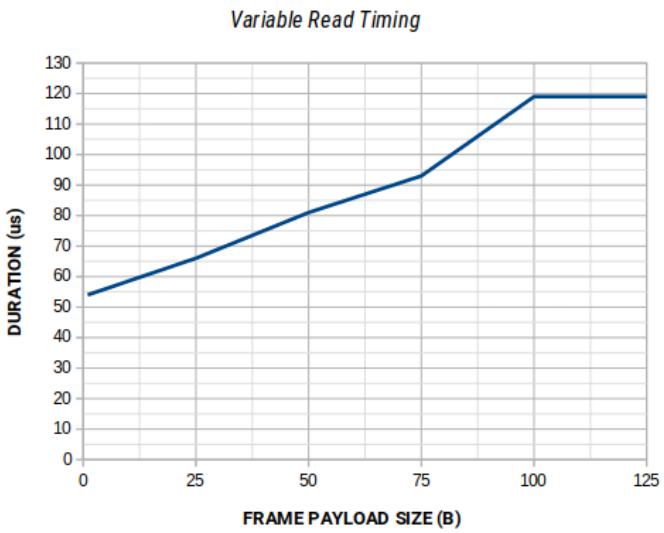
1. STM32 FMC Test Conditions :

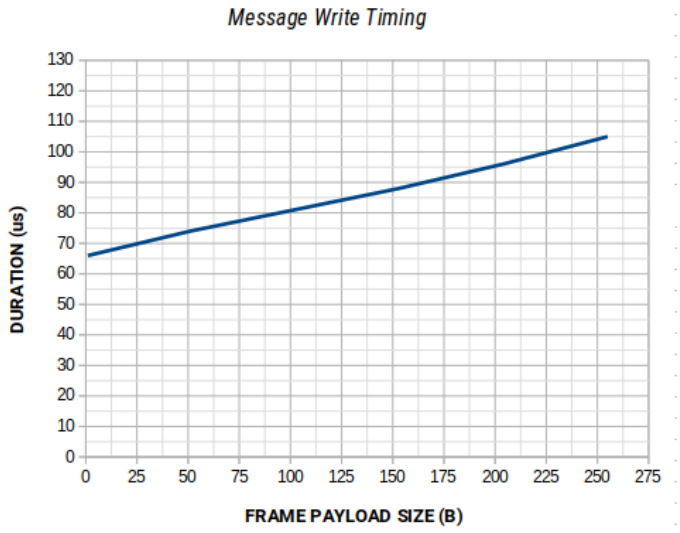
STM32 FMC Configuration [DEV_BOARD TEST]	
FMC Clock	100MHz
AddressSetupTime	5
AddressHoldTime	1

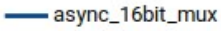
DataSetupTime	10
BusTurnAroundDuration	0
Capacitive Load CL	30 pF

8.3 Read/Write Performance









Notes:

- These graphs are taken from the POWERFIP API performance measurement. Respectively the functions: *pwrfip_var_write()*, *pwrfip_var_read()*, *pwrfip_msg_write()*.

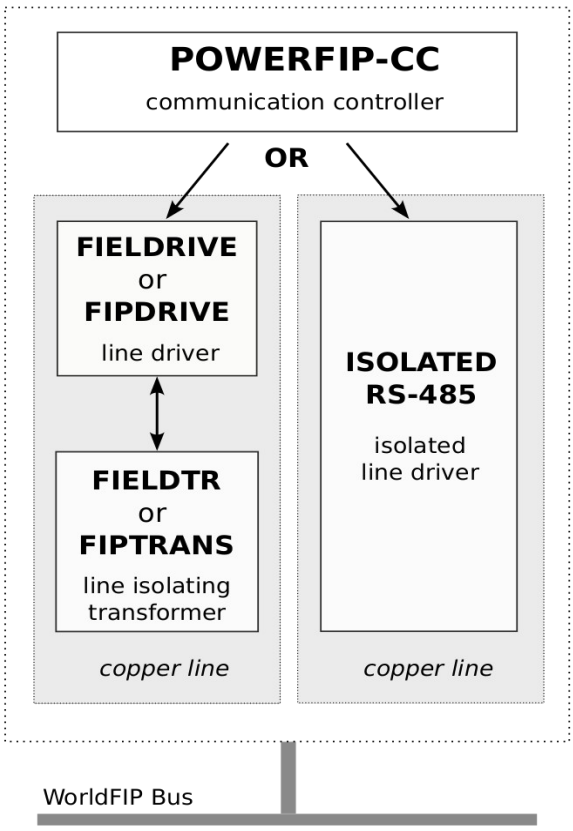
9 MAU Interface

Medium Attachment Unit coupling interface mode selection is performed through a dedicated input pin : *MAU_CFG*

Message Attachment Unit Configuration

MAU_CFG	
Value	Description
0	Alstom's transceiver (FielDrive™) or Exoligent's transceiver (FipDrive)
1	Generic RS-485 transceiver

POWERFIP-CC can interface with several WorldFIP line drivers :



- **FIELDRIVE ™:**

  Historically, FIP physical lines were designed using Alstom's FielDrive™ component. It was a fully integrated driver designed to interface a protocol component to a twisted copper pair through an isolating transformer (IEC 61158-2). This circuit incorporated additional output signals such as *RX Carrier Detection* (CDn), *Transmit Symbol Checkup + Line Overload/Underload Detection* (TXER), and *Jabber Inhibit Watchdog* (WDGn).

  Although End-Of-Life of this component was fixed for 2024, POWERFIP-CC supports it. To use it, set MAU_CFG input pin to 0.

- **FIPDRIVE** :

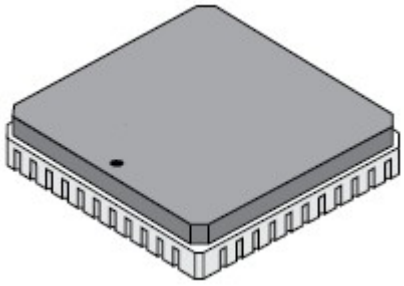
  Following the discontinuation of Alstom's FieldDrive™ product (End-Of-Life : 2024), Exoligent developed FipDrive component, a pin-to-pin compatible circuit. To use this MAU interface, set MAU_CFG input pin to 0.

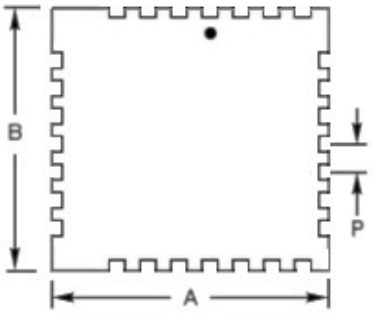
- **ISOLATED RS-485** :

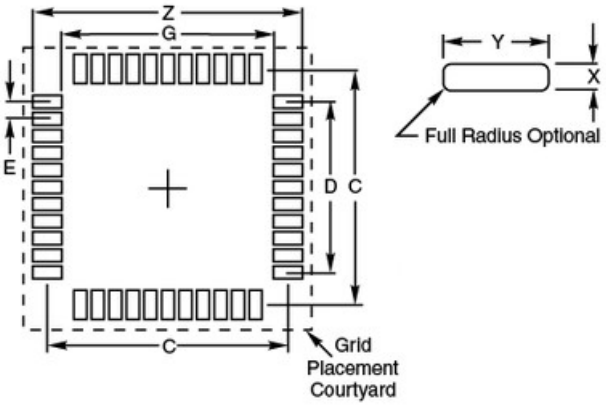
  By configuring the POWERFIP-CC with the MAU_CFG input pin to 1, the additional FieldDrive™ signals are rebuilt directly inside the chip carrier. In this mode, instead of being configured as inputs for the POWERFIP-CC, the CD#, TXER and WDG# pins are automatically set as outputs to use these signals on the board level.

  So, the chip can now be interfaced with most isolated RS-485 transceivers.

10 Mechanical, Packaging Information







Chip Carrier Compoment Dimensions

Component Identifier	A (mm)		B (mm)		P (mm)
	Min	Max	Min	Max	Basic
CC-84	29.21	29.41	29.21	29.41	1.27

Chip Carrier Footprint Pattern

Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm)	C (mm)	D (mm)	E (mm)	Placement Grid (mm x mm)
				Ref	Ref	Ref	Ref	
CC-84	30.57	26.42	0.70	2.00	28.45	25.40	1.27	31.3 x 31.3

11 Application Notes

11.1 Terms, abbreviations and definitions

Term	Description
ACK	Acknowledge
ALE	Address Latch Enable
API	Application Programming Interface
BA	Bus Arbiter
CC	Chip Carrier
CD	Carrier Detect
CMD	Command
CS	Chip Select
EBI	External Bus Interface
FIP	Factory Instrumentation Protocol
FPGA	Field Programmable Gate Arrays
FSN	Factory Serial Number
FW	Firmware
GW	Gateware
IC	Integrated Circuit
INT	Interrupt
IO	Input/Output Data
IRQ	Interrupt Request
JTAG	Joint Test Action Group
LSAP	Link Service Access Point
LSB	Least Significant Bit or Byte
LVTTL	Low Voltage TTL (Transistor-Transistor Logic)
MAU	Medium Attachment Unit
MBX	MailBox
MPS	Manufacturing Periodic/aperiodic Services
MSB	Most Significant Bit or Byte
OE	Output Enable
PLC	Programmable Logic Controller
QFP	Quad Flat Package
RDY	Ready

SM-MPS	System Management Manufacturing Periodic/aperiodic Services
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
UID	Unique Identifier
WDG	Watchdog
WE	Write Enable

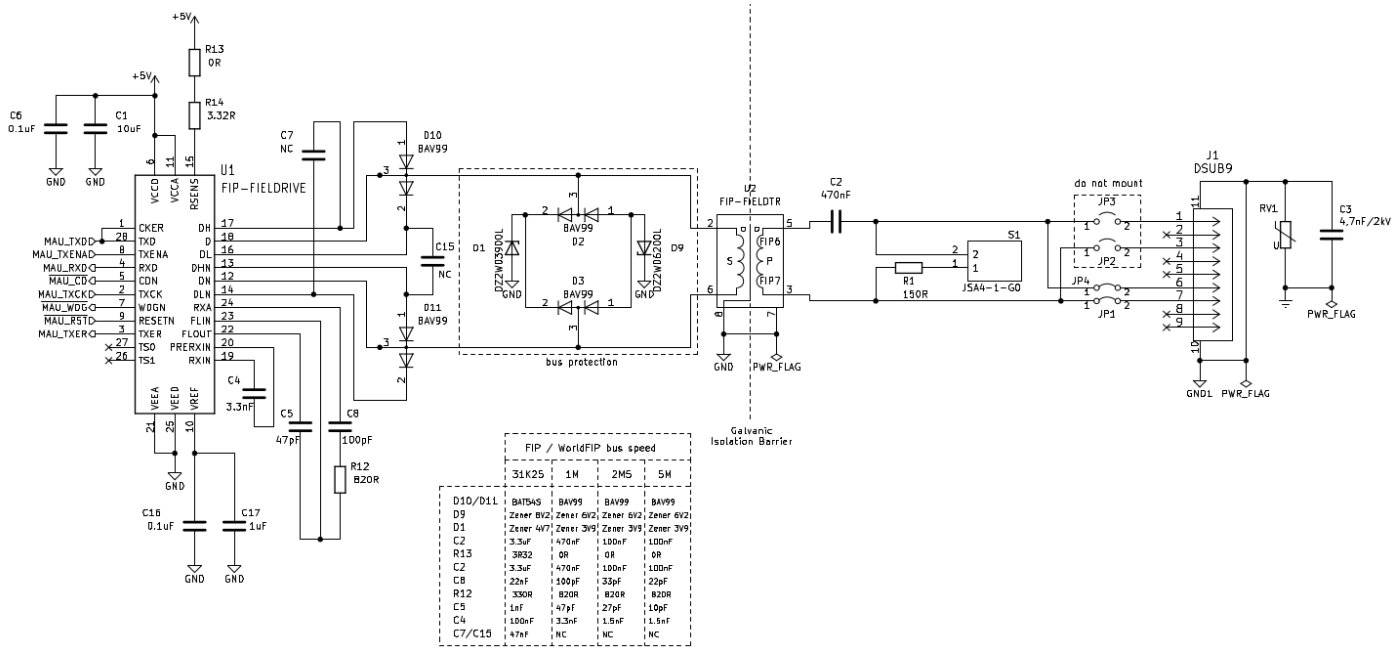
11.2 Resources

Additional Resources

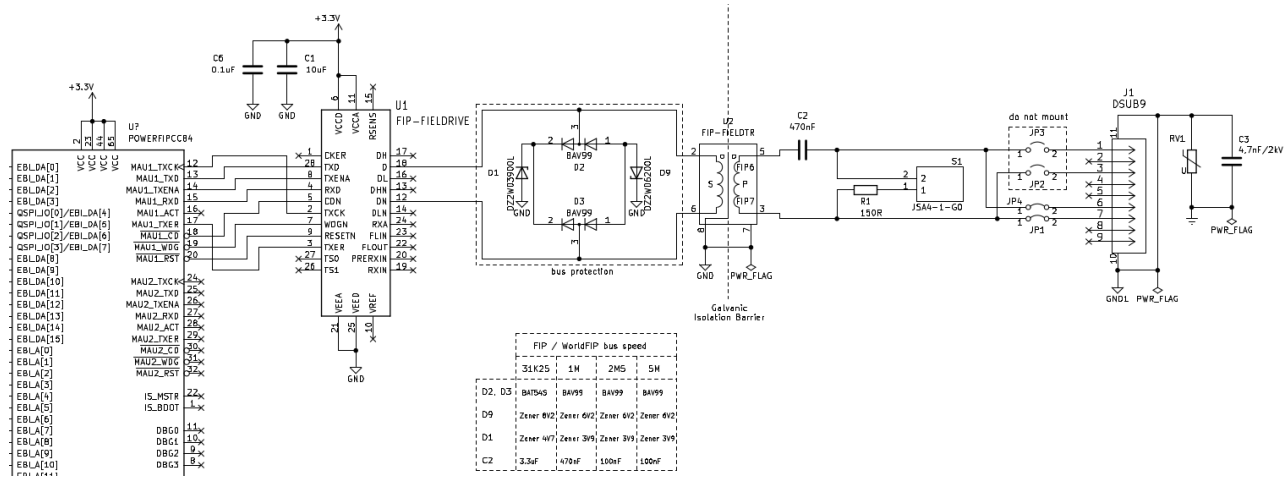
Official Website	www.exoligent.com
API Reference	https://www.exoligent.com/wiki/worldfip/pwrfip/library.html
Development Board	https://www.exoligent.com/en/chips-fip/103-powerfip-cc84-dev-board.html
FipDrive	https://www.exoligent.com/fr/chips-fip/89-fipdrive-ex-fieldrive.html
FielDrive	https://www.exoligent.com/img/cms/produits/WorldFIP/fip-chips/fieldrive/fieldrive-rev200611.pdf
FieldTR	https://www.exoligent.com/img/cms/produits/WorldFIP/fip-chips/fieldtr/fieldTR-rev200701.pdf
E-mail (Technical Support)	info@exoligent.com

11.3 Interfacing with the Line Transceiver

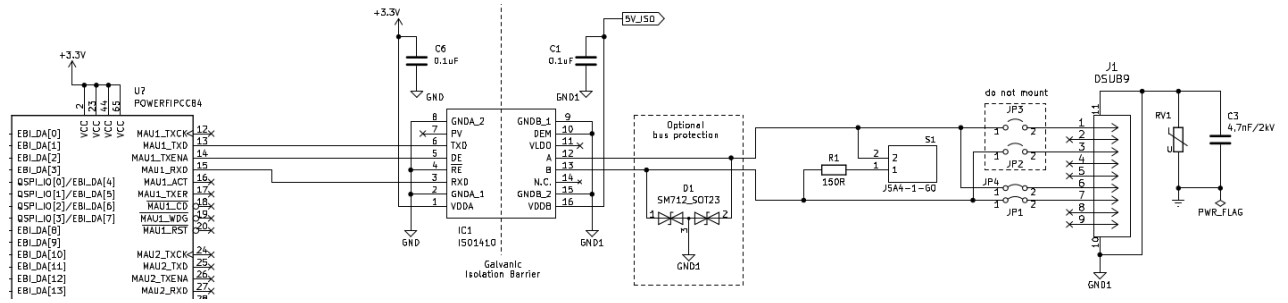
11.3.1 Alstom's FielDrive



11.3.2 Exoligent's FipDrive



11.3.3 Generic RS-485 drivers



11.4 Reflow Profile Guideline