WORLDFIP MEDIUM ATTACHMENT UNIT

JANUARY 2025

1 Features

- WorldFIP/FIP physical layer
  - IEC 61158-2
  - EN 50170
  - Bitrate support : 1Mbps, 2.5Mbps, 5Mbps
- LVTTL compatible inputs and outputs
- Bus I/O protection
  - ± 70V DC bus fault
  - ± 16kV HBM ESD
  - ± 12kV IEC 61000-4-2 contact discharge
  - ± 12kV IEC 61000-4-2 air-gap discharge
  - ± 4kV IEC 61000-4-4 fast transcient burst
- Half-duplex device
- Single power supply
  - 3V to 5.5V supply voltage
- Dimensions (L x W x H)
  - 11 x 11 x 5.2 mm
- Contacting / Pinout
  - 28 solder contacts 1mm with 1.27mm grid
  - PLCC-28 footprint compliant
- Operating temperature
  - -40°C to +100°C
- Lead-free available
- Designed in France

3 Applications

- Fieldbus networks
- Factory automation and control

2 Description

The *EXOLIGENT* FIPDRIVE Chip Carrier is a integrated line driver circuit providing the interface between a protocol component and an isolating transformer of a fieldbus physical medium (MAU) operating on a single 3V to 5.5V supply.

This component implements physical layer specification following standards : IEC 61158-2, EN50170.

This device is pin-to-pin compatible with Alstom's FielDrive™ component (End-Of-Life: 2024) to ensure compatibility between the two components and perpetuate existing designs.

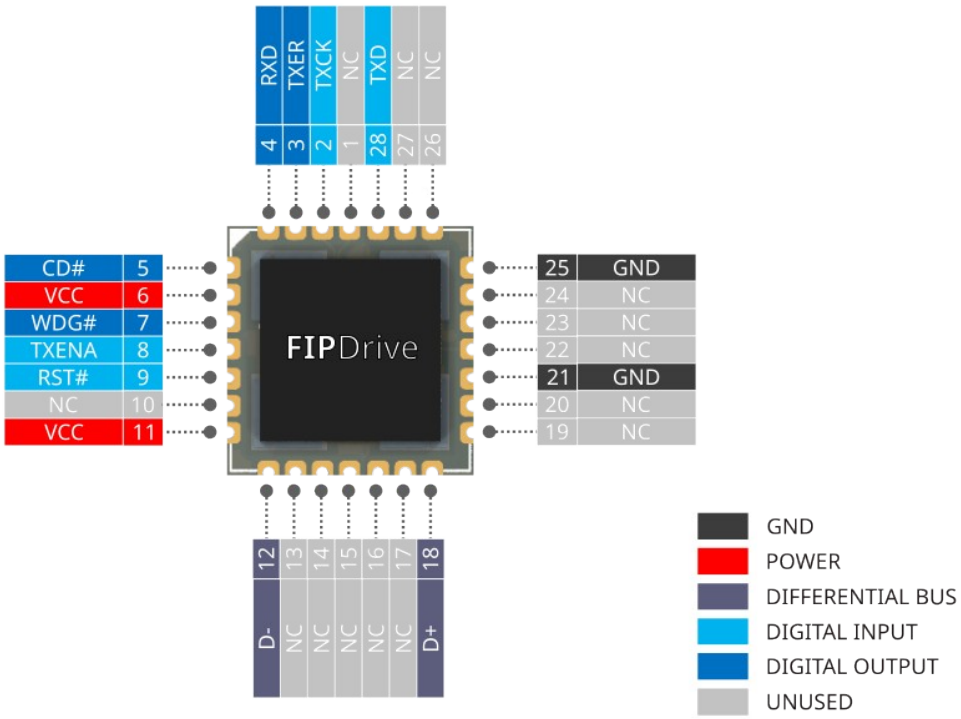
FIPDRIVE PCB footprint is PLCC-28 compliant.

Table of Contents

4 Revision History

Revision	Changes	Authors	Date
Rev.A	Initial Version	MC	1/25

5 Pin Configuration and Functions



Pin Descriptions

Pin Number	Pin Name	Type	Description
1	-	-	Not connected
2	TXCK	I	Half bit clock[1]
3	TXER	O	Transmit error
4	RXD	O	Received data
5	CD#	O	Reception activity detection
6	VCC	PWR	Positive supply voltage
7	WDG#	O	Watchdog on transmitter
8	TXENA	I	Transmitter enable
9	RST#	I	Initialization control
10	-	-	Not connected
11	VCC	PWR	Positive supply voltage
12	D-	I/O	Bus I/O port, D- (complementary to D+)

Pin Number	Pin Name	Type	Description
13	-	-	Not connected
14	-	-	Not connected
15	-	-	Not connected
16	-	-	Not connected
17	-	-	Not connected
18	D+	I/O	Bus I/O port, D+ (complementary to D-)
19	-	-	Not connected
20	-	-	Not connected
21	GND	PWR	Negative supply voltage (0V)
22	-	-	Not connected
23	-	-	Not connected
24	-	-	Not connected
25	GND	PWR	Negative supply voltage (0V)
26	-	-	Not connected
27	-	-	Not connected
28	TXD	I	Transmitter data

Notes:

1. 500ns@1Mbps, 200ns@2.5Mbps, 100ns@5Mbps

6 Specifications

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.5	7	V
V_{DC}[1]	DC Bus Voltage	-70	70	V
V_{IN}	Input Voltage	-0.3	V_{CC} + 0.3	V
T_{stg}	Storage Temperature	-65	+150	°C
T_{amb}	Ambient Temperature	-40	+100	°C
T_J	Junction Temperature	-	+150	°C

Notes:

- Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All voltages referenced to GND.
- (1) : Range at any bus pin (D+ or D-) as differential or common-mode with respect to GND.

6.2 ESD Ratings

				Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus terminals	± 16,000	V
			All pins except bus terminals	± 2,000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	Bus terminals	± 1,500	V
			All pins except bus terminals	± 1,000	V

Notes:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

				Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals	± 12,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals	± 12,000	V
V(EFT)	Electrical fast transcient	Per IEC 61000-4-4	Bus terminals	± 4,000	V

6.4 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3	-	5.5	V
V_{IN}	Input Voltage	0	-	V_{CC}	V
T_{amb}	Ambient Temperature (in free air)	-40	-	+100	°C
T_J	Junction Temperature	-40	-	+125	°C

6.5 Electrical Characteristics

Logic Section Part 1[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage		-0.3	-	0.8	V
V_{IH}	High-level input voltage		2.0	-	3.5	V
V_{OL}	Low-level ouput voltage		-	-	0.4	V
V_{OH}	High-level output voltage		2.9	-	-	V
I_{OL}	Low-level ouput current		8	-	-	mA
I_{OH}	High-level output current		-	-	-8	mA
I_{IL}, I_{IH}[2]	Input or I/O Leakage current	$0 \le V_{IN} \le 3.5$ V	-10	-	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 2.145$ V	-11	-	-172	µA
C_{IN}[3]	I/O Capacitance	V_{CC} = 3.3V, V_{IO} = 0 to 3.5V	-	6	-	pF

Logic Section Part 2[4]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage		-	-	0.8	V
V_{IH}	High-level input voltage		2.0	-	-	V
V_{OL}	Low-level ouput voltage		-	-	0.55	V
V_{OH}	High-level output voltage		2.3	-	-	V
I_{OL}	Low-level ouput current		24	-	-	mA
I_{OH}	High-level output current		-	-	-24	mA
C_{IN}	I/O Capacitance	V_{CC} = 3.3V	-	4	-	pF

Notes:

1. TXER, WDG#, CD# pins (fixed by FPGA)
2. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.
3. T_A 25 °C, f = 1.0 MHz.
4. RXD, TXD, TXENA, TXCK, RST# pins (fixed by the Level Translator)

7 Detailed Description

7.1 Overview

FIPDRIVE is a top-side mounted circuit board in the compact dimensions of 11x11 mm and will be soldered to the baseboard. As for a QFP part the solder pads are located on the side and enables an easy handling.

The implementation of complete line driving/receiving circuitry requires associating the FIPDRIVE chip with :

- An isolating transformer
- A protection circuit

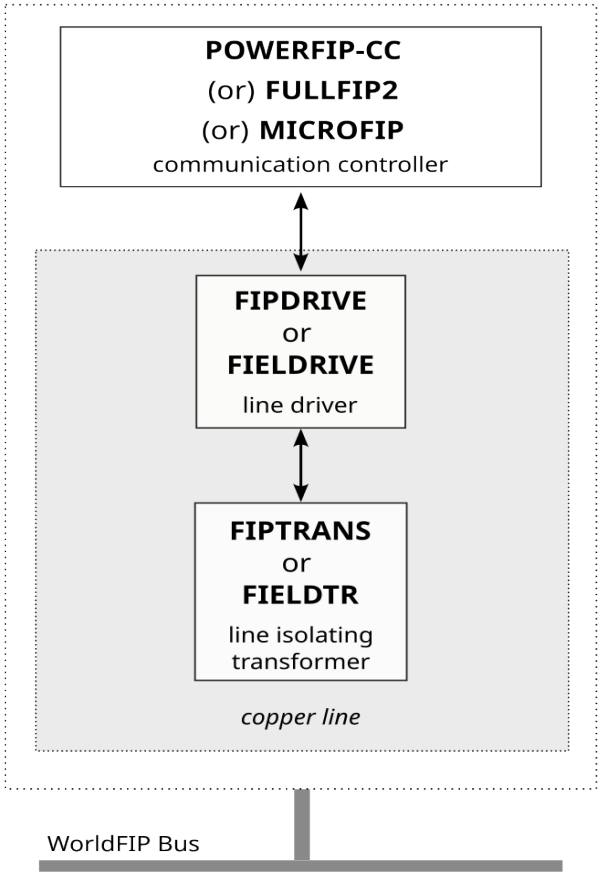
The FIPDRIVE component integrates a line transceiver, an activity monitoring of the transceiver and a FPGA to generate additionnal output signals such as *RX Carrier Detection (CD#), Transmit Symbol Checkup + Line Overload/Underload Detection (TXER), and Jabber Inhibit Watchdog (WDG#)*.

The FIPDRIVE component is designed to be connected with a protocol coprocessor (POWERFIP-CC, FULLFIP2, MICROFIP…).

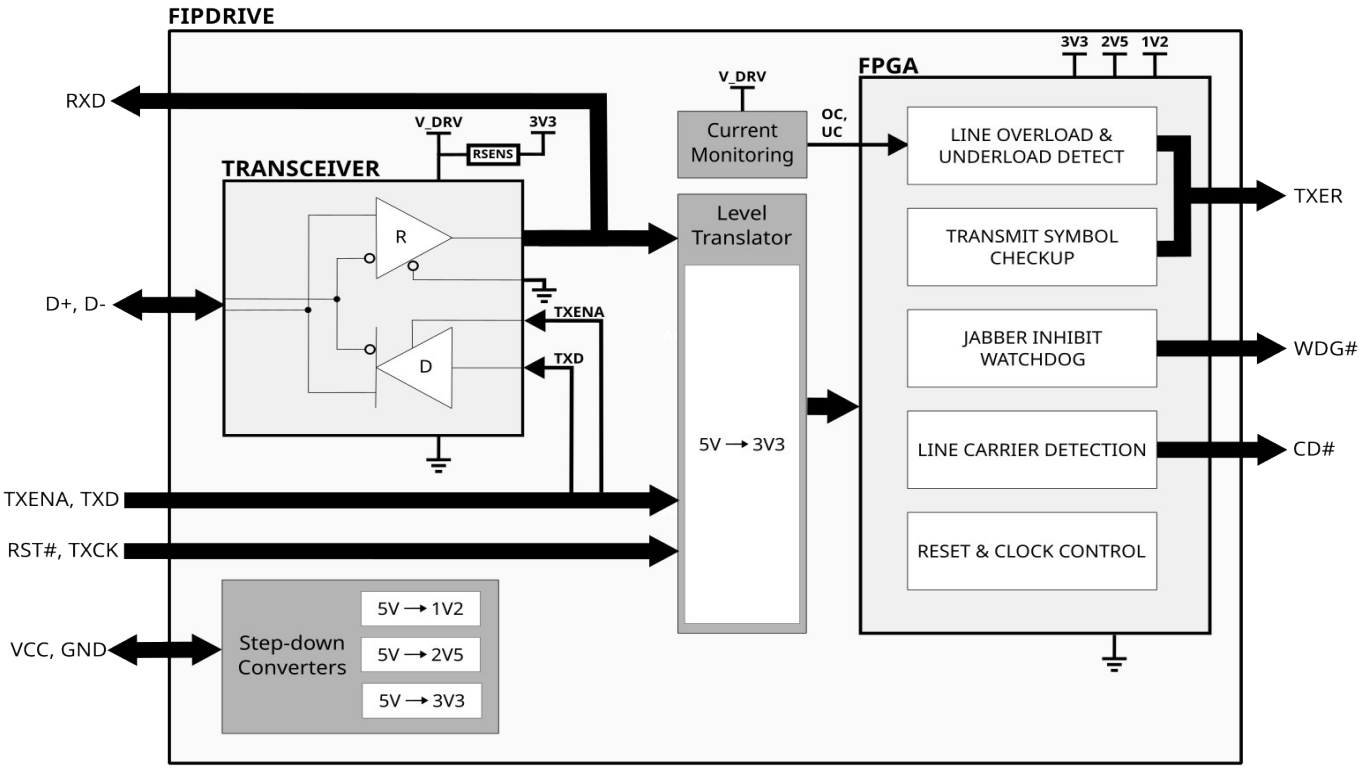
The chip supports the following FIP bitrates values : 1Mbps, 2.5Mbps and 5 Mbps.

The transmit and receive signals on the network interface are encoded data sequence (Manchester Biphase L).

WorldFIP Fieldbus Subscriber Connection



7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ±70-V Fault Protection

The FIPDRIVE's transceiver has extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, FIPDRIVE device is protected up to ±70 V without the need for any external components.

7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

7.3.3 Driver Overvoltage and Overcurrent Protection

The FIPDRIVE's driver is protected against any DC supply shorts in the range of -70 V to +70 V. The device internally limits the short circuit current to ±250 mA in order to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5 mA if the output fault voltage exceeds |±25 V|.

7.3.4 Enhanced Receiver Noise Immunity

The differential receiver of FIPDRIVE features fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis ensures excellent noise immunity.

7.3.5 Receiver Fail-Safe Operation

The FIPDRIVE's receiver is fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

7.3.6 Line Carrier Detection

Internal digital processing of the received signal consists in sampling the signal on alternate asynchronous clock edges in order to determine if the incoming signal is valid or is a glitch. A valid signal will produce a carrier detect output (*CD#*).

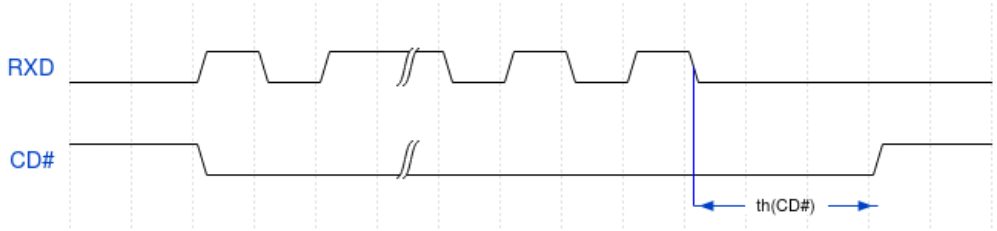
7.3.7 Transmit Error Detection

FIPDRIVE's driver stage manages four basic functions :

- The FIPDRIVE's driver is controlled by the *TXENA* input signal. When *TXENA* is disabled, the driver switches to high-impedance to prevent the controller from interfering with the line.
- A *TXER* signal is generated when the symbol duration exceeds $\mathbf{t_{Dsymb}}$, indicating a « *stuck at fault* » condition.
- A *TXER* signal is generated when the overload or underload condition is detected from the driver output.
- A watchdog signal *WDG#* is generated when the frame length exceeds $\mathbf{t_{Djab}}$, the jabber time. The signal remains active until the chip is reset with the *RST#* input signal.

7.4 Timing Considerations

7.4.1 Carrier Detection (CD#)

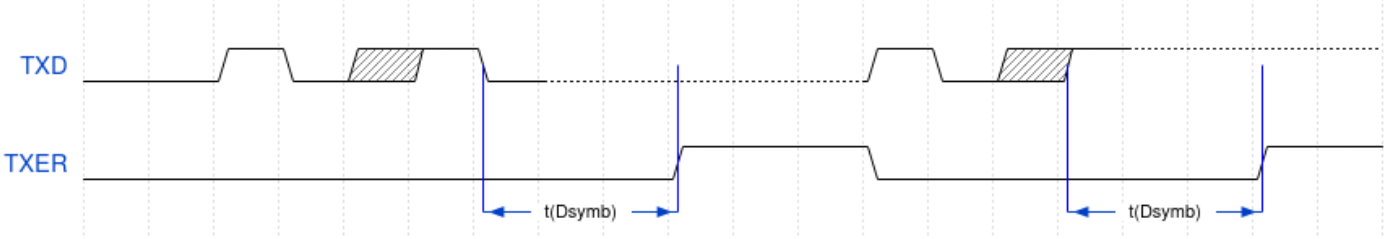


Symbol	Description	Min	Typ	Max	Unit
$t_{h(CD\#)}$	CD# hold time after RXD low	3	3.5	4	T_{Bit}[1]

Notes:

1. T_{Bit} = 1us@1Mbps, 400ns@2.5Mbps, 200ns@5Mbps

7.4.2 Transmit Symbol Checkup (TXER)

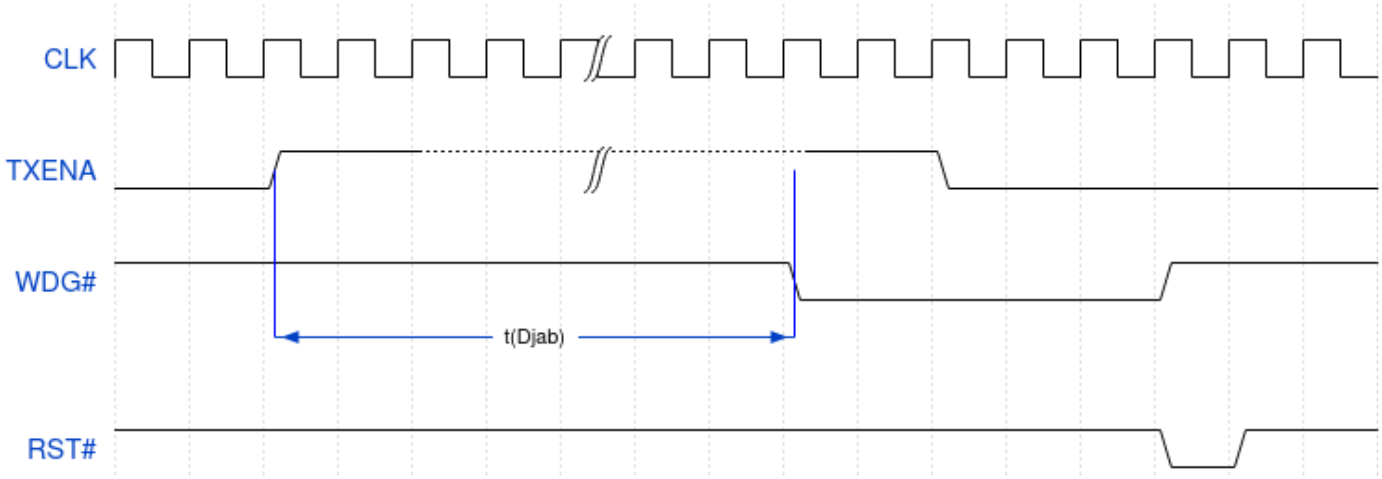


Symbol	Description	Min	Typ	Max	Unit
t_{Dsymb}	Fault symbol time	-	4	-	T_{Bit}[1]

Notes:

1. T_{Bit} = 1us@1Mbps, 400ns@2.5Mbps, 200ns@5Mbps

7.4.3 Jabber Inhibit Watchdog (WDG#)

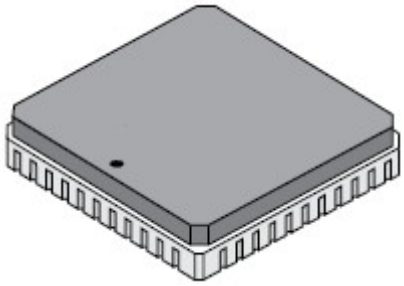


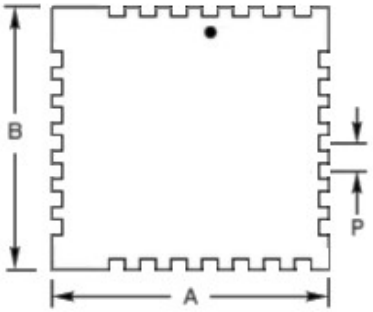
Symbol	Description	Min	Typ	Max	Unit
t_{Djab}	Fault jabber time	-	8192	-	T_{Bit}[1]

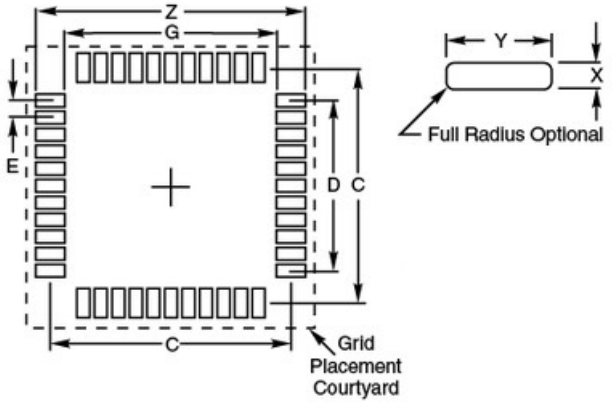
Notes:

1. T_{Bit} = 1us@1Mbps, 400ns@2.5Mbps, 200ns@5Mbps

8 Mechanical, Packaging Information







Chip Carrier Compoment Dimensions

Component Identifier	A (mm)		B (mm)		P (mm)
	Min	Max	Min	Max	Basic
CC-28	11.43	11.58	11.43	11.58	1.27

Chip Carrier Land Pattern

Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm)	C (mm)	D (mm)	E (mm)	Placement Grid (mm x mm)
				Ref	Ref	Ref	Ref	
CC-28	13.40	9.00	0.60	2.20	11.20	7.62	1.27	30 x 30

9 Application Notes

9.1 Terms, abbreviations and definitions

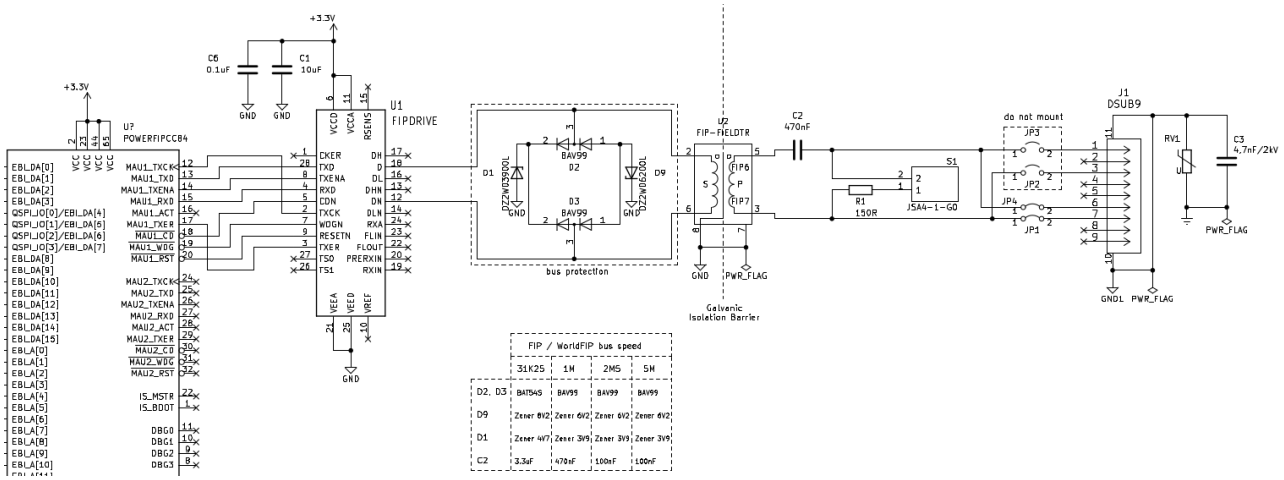
Term	Description
CC	Chip Carrier
CD	Carrier Detect
FIP	Factory Instrumentation Protocol
FPGA	Field Programmable Gate Arrays
IC	Integrated Circuit
IO	Input/Output Data
LVTTL	Low Voltage TTL
MAU	Medium Attachment Unit
QFP	Quad Flat Package
TTL	Transistor-Transistor Logic
WDG	Watchdog

9.2 Resources

Additional Resources

Official Website	www.exoligent.com
PowerFIP-CC	https://www.exoligent.com/wiki/worldfip/pwrfip/POWERFIPCC_Datasheet.pdf
FipDrive	https://www.exoligent.com/wiki/worldfip/pwrfip/FIPDRIVE_Datasheet.pdf
E-mail (Technical Support)	info@exoligent.com

9.3 FIPDRIVE Interfacing

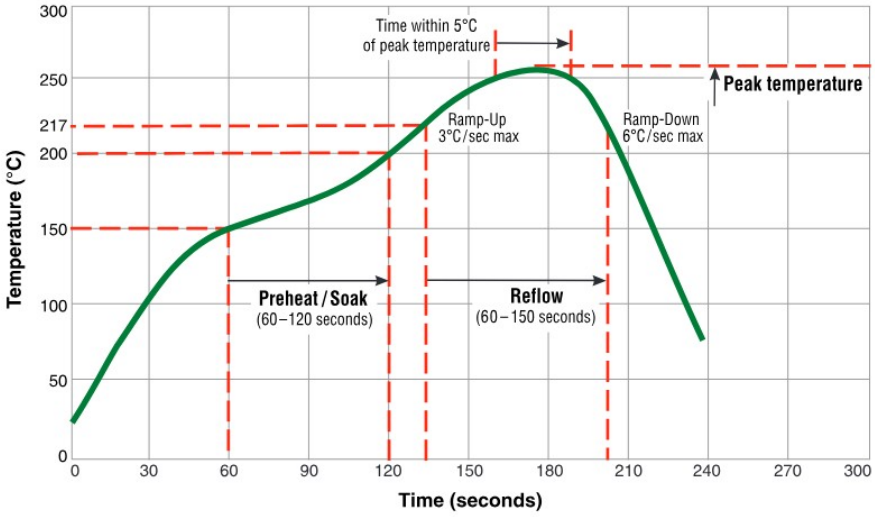


Part	Connection	Function
POWERFIP-CC[1] [controller]	With the line driver	Ensures data exchange and real-time fieldbus communication
FIPDRIVE[2] [line driver]	Between the controller and the transformer	Adapts the communication controller's I/O signals to the differential bus
FIPTRANS[3] [transformer]	Between the transformer and the connector	Ensures galvanic isolation and avoids transformer saturation by en eventual continuous current
DSUB-9 [connector]	With the external bus	The physical layer standard for interfacing with fieldbus

Notes:

1. POWERFIP-CC is a replacement part for ALSTOM's FULLFIP2 and MICROFIP (End-Of-Life).
2. FIPDRIVE is a replacement part for ALSTOM's FIELDRIVE (End-Of-Life). Pin-to-pin compatible.
3. FIPTRANS is a replacement part for ALSTOM's FIELDTR (End-Of-Life). Pin-to-pin compatible.

9.4 Reflow Profile Guideline



Description	Value	Unit
Preheat / Soak Temperature	150 – 200	°C
Preheat / Soak Duration	60 – 120	seconds
Ramp-up Rate	3	°C/second
Typ. Reflow Temperature	217	°C
Peak Temperature	255 – 260	°C
Time Within 5 °C of Peak	30	seconds
Time Above Reflow Temperature	60 – 150	seconds
Ramp-down Rate	6	°C/second